THE INVENTION CLAIMED IS

1. A wireless computer data network, comprising:

a plurality of mobile, wireless appliances;

at least one base station connected to the Internet; and

an interface circuit for establishing an ad-hoc radio communication link amongst the plurality of mobile, wireless appliances and the base station;

wherein, the interface circuit operates with carrier frequencies in the 5GHz band and data is transferred with orthogonal frequency division multiplexing (OFDM).

2. The network of claim 1, wherein each of the plurality of mobile, wireless appliances comprises:

a single integrated circuit that implements a complete radio transceiver for wireless connection with the interface circuit.

3. The network of claim 2, wherein said single integrated circuit comprises:

at least two independent frequency synthesizers connected in a double-conversion superheterodyne configuration.

4. The network of claim 2, wherein said single integrated circuit comprises:

a pair of on-chip synthesizers are included that each have a voltage-controlled oscillator and phase-locked loop that can be operated independently for each conversion stage, or operated in offset mode; and

an input is provided for bypassing the on-chip synthesizers and to inject external reference frequencies during voltage-controlled oscillator and phase-locked loop testing, chip characterization, and automatic compensation modeling.

5. A wireless computer data network that includes a plurality of untethered mobile units that provide for ad-hoc data connections with an Internet-connected base station using the IEEE-802.11a standard;

wherein, each mobile unit and base station includes a radio transceiver fully integrated on a single semiconductor chip with a double-conversion superheterodyne type receiver portion and a two-stage up-conversion transmitter that shares the same intermediate and local oscillator frequencies;

wherein, a pair of on-chip synthesizers are included that each have a voltage-controlled oscillator and phase-locked loop that can be operated independently for each conversion stage, or operated in offset mode; and

wherein, an input is provided for injecting external reference frequencies during voltage-controlled oscillator and phase-locked loop testing, chip characterization, and automatic compensation modeling.

6. A wireless communication system, comprising:

a physical layer interface (PHY) that includes an antenna for 5GHz carrier service, a transmit/receive (T/R) switch for half-duplex operation, a low-noise amplifier (LNA), a power amplifier (PA), a radio frequency (RF) transceiver, and a data modem;

an IEEE-802.11-compliant media access controller (MAC) for ISO-defined layer-2 processing; and

a static random access memory (SRAM) for data buffering and program storage.

7. The system of claim 6, further comprising:

a PCMCIA wireless LAN card on which the PHY, MAC, and SRAM are fully disposed;

wherein the LAN card is constructed on a single printed circuit board (PCB) and the RF transceiver and modem are each implemented with CMOS technology in individual integrated circuits.

8. The system of claim 6, wherein:

said RF transceiver and modem constitute a complete wireless engine for OSI-defined layer-1 physical layer (PHY) functionality in broadband wireless local area networks.

9. A single-chip radio transceiver for operation in the 5GHz radio spectrum, comprising:

a double-conversion superheterodyne radio receiver;

a two-stage up-conversion radio transmitter;

a first frequency synthesizer connected to supply a higher local oscillator reference frequency to both the receiver and transmitter;

a second frequency synthesizer independent of the first frequency synthesizer, and connected to supply a lower local oscillator reference frequency to both the receiver and transmitter;

a plurality of ramp and bias generators for selectively and gradually applying operating power to various parts of the receiver, transmitter, and the first and second frequency synthesizers; and

a microcomputer connected to monitor and control each of the plurality of ramp and bias generators, receiver, transmitter, and the first and second frequency synthesizers.

10. The single-chip radio transceiver of claim 9, wherein:

the microcomputer compensates for manufacturing production variations by adjustments output to the plurality of ramp and bias generators.

11. The single-chip radio transceiver of claim 9, wherein:

the microcomputer compensates for temperature variations according to device characteristic models.

12. The single-chip radio transceiver of claim 9, further comprising:

an input provided for injecting an external reference frequency during voltage-controlled oscillator and phase-locked loop testing, chip characterization, and automatic compensation modeling;

wherein, the microcomputer thereafter compensates during device operation for production and temperature variations.

13. A wireless computer data network, comprising:

a wireless appliance means for mobile roaming within reach of an ad-hoc wireless communication link;

at least one base station means for connecting the wireless appliance means through to the Internet over said ad-hoc wireless communication link; and

an interface means for establishing said ad-hoc radio communication link, and for operating with carrier frequencies in the 5GHz band, and for transferring orthogonal frequency division multiplexing (OFDM) data.

14. The network of claim 13, wherein each of the wireless appliance means comprises:

a single integrated circuit means for implementing a single radio transceiver portion of the interface means.

15. The network of claim 14, wherein said single integrated circuit means comprises:

at least two independent frequency synthesizers means for connection in a double-conversion superheterodyne configuration.

16. The network of claim 14, wherein said single integrated circuit means comprises:

a pair of on-chip synthesizer means for voltage-controlled oscillator and phase-locked loop functions that can be operated independently for each conversion stage, or operated in offset mode; and

an input means for bypassing the on-chip synthesizers and to inject external reference frequencies during voltage-controlled oscillator and phase-locked loop testing, chip characterization, and automatic compensation modeling.

17. A method of operating a wireless computer data network that includes a plurality of untethered mobile units that provide for ad-hoc data connections with an Internet-connected base station using the IEEE-802.11a standard, the method comprising the steps of;

completely integrating a radio transceiver in each mobile unit and base station on a single semiconductor chip with a double-conversion superheterodyne type receiver portion and

a two-stage up-conversion transmitter that shares the same intermediate and local oscillator frequencies;

including a pair of on-chip synthesizers on said chip that each have a voltage-controlled oscillator and phase-locked loop that can be operated independently for each conversion stage, or operated in offset mode; and

providing an input for injecting external reference frequencies during voltage-controlled oscillator and phase-locked loop testing, chip characterization, and automatic compensation modeling.

18. A wireless communication system, comprising:

means for a physical layer interface (PHY) that includes an antenna for 5GHz carrier service, means for a transmit/receive (T/R) switch for half-duplex operation, means for a low-noise amplifier (LNA), means for a power amplifier (PA) 208, means for a radio frequency (RF) transceiver, and means for a data modem 212;

means for an IEEE-802.11-compliant medium access controller (MAC) for ISO-defined layer-2 processing; and

means for a static random access memory (SRAM) for data buffering and program storage.

19. The system of claim 18, further comprising:

means for a PCMCIA wireless LAN card on which the PHY, MAC, and SRAM are fully disposed;

wherein the LAN card is constructed on a single printed circuit board (PCB) and the RF transceiver and modem are each implemented with CMOS technology in individual integrated circuits.

20. The system of claim 18, wherein:

said RF transceiver and modem means constitute a complete wireless engine for OSI-defined layer-1 physical layer (PHY) functionality in broadband wireless local area networks.

21. A single-chip radio transceiver for operation in the 5GHz radio spectrum, comprising:

means for a double-conversion superheterodyne radio reception;

means for a two-stage up-conversion radio transmission;

means for synthesizing and connecting a first frequency synthesizer to supply a higher local oscillator reference frequency to both the reception and transmission means;

means for connecting a second frequency synthesizer independent of the first frequency synthesizer, and for connecting to supply a lower local oscillator reference frequency to both the receiver and transmitter;

ramp and bias generator means for selectively and gradually applying operating power to various parts of the receiver, transmitter, and the first and second frequency synthesizers; and

microcomputer means for monitoring and controlling ramp and bias generator means, the reception and transmission means, and said first and second frequency synthesizers.

22. The single-chip radio transceiver of claim 21, wherein:

the microcomputer means includes means for compensating any manufacturing production variations by adjusting an output provided to the ramp and bias generator means.

23. The single-chip radio transceiver of claim 21, wherein:

the microcomputer means compensates for temperature variations according to device characteristic models.

24. The single-chip radio transceiver of claim 21, further comprising:

an input means for injecting an external reference frequency during voltage-controlled oscillator and phase-locked loop testing, chip characterization, and automatic compensation modeling;

wherein, the microcomputer means thereafter compensates during device operation for production and temperature variations.